IN THE CLAIMS:

Please amend claims 1, 13, 19, and 25-28 as indicated below.

1. (Currently Amended) A memory controller, comprising:

an array of tag address storage locations; and

a command sequencer and serializer unit coupled to the array of tag address storage locations to receive information regarding whether there is a cache hit from the array of tage address storage locations, the command sequencer and serializer unit to control a data cache located on a memory module using the received information, the command sequencer and serializer unit to control the data cache located on the memory module by delivering a plurality of commands over a plurality of command and address lines, the commands sequentially delivered over a plurality of transfer periods of a memory access transaction and each command being delivered within one of the transfer periods, the plurality of commands including an activate command and a cache fetch command, the activate and cache fetch commands differing in format only in the information delivered during a last transfer period of the plurality of transfer periods.

2. (Previously Presented) The memory controller of claim 1, the activate command and the cache fetch command differing in cache hit information delivered during the last transfer period.

3. (Previously Presented) The memory controller of claim 2, the cache fetch command further including way information delivered during the last transfer period.

4. (Previously Presented) The memory controller of claim 3, the plurality of commands each delivered over four transfer periods.

5. (Previously Presented) The memory controller of claim 4, the activate and cache fetch commands each including memory module destination information during a first transfer period.

6. (Previously Presented) The memory controller of claim 5, the activate and cache fetch commands each including row address information during each of the four transfer periods.

7. (Previously Presented) The memory controller of claim 1, the plurality of commands further including a read command and a read and preload command, the read and read and preload commands differing in format only in the information delivered during a last transfer period.

8. (Previously Presented) The memory controller of claim 7, the read command and read and preload command differing in cache hit information delivered during the last transfer period.

9. (Previously Presented) The memory controller of claim 8, the read and preload command further including way information delivered during the last transfer period.

10. (Previously Presented) The memory controller of claim 9, the plurality of commands each delivered over four transfer periods.

11. (Previously Presented) The memory controller of claim 10, the read command and the read and preload command each including memory module destination information during a first transfer period.

12. (Previously Presented) The memory controller of claim 11, the read command and read and preload command each including column address information during each of the four transfer periods.

13. (Currently Amended) A memory module, comprising:

at least one memory device; and

a data cache coupled to the memory device, the data cache controlled by a plurality of commands delivered by a memory controller component over a plurality of command lines of a memory bus, the memory controller component including an array of tag address storage locations, the commands sequentially delivered over a plurality of transfer periods of a memory access transaction, the plurality of commands including an activate command and a cache fetch command, the activate and cache fetch commands differing in format only in the information delivered during a last transfer period of the plurality transfer periods.

14. (Previously Presented) The memory module of claim 13, the activate command and the cache fetch command differing in cache hit information delivered during the last transfer period.

15. (Previously Presented) The memory module of claim 14, the cache fetch command further including way information delivered during the last transfer period.

16. (Previously Presented) The memory module of claim 15, the plurality of commands each delivered over four transfer periods.

17. (Previously Presented) The memory module of claim 16, the activate and cache fetch commands each including memory module destination information during a first transfer period.

18. (Previously Presented) The memory module of claim 17, the activate and cache fetch commands each including row address information during each of the four transfer periods.

19. (Currently Amended) A system, comprising:

a processor;

a memory controller coupled to the processor, the memory controller including

an array of tag address storage locations, and

a command sequencer and serializer unit coupled to the array of tag address storage locations; and

a memory module coupled to the memory controller via a memory bus, the memory module including

at least one memory device, and

a data cache coupled to the memory device, the data cache controlled by a plurality of commands delivered by the memory controller, the

commands sequentially delivered over a plurality of transfer periods of a memory access transaction, the plurality of commands including an activate command and a cache fetch command, the activate and cache fetch commands differing in format only in the information delivered during a last transfer period of the plurality of transfer periods.

20. (Original) The system of claim 19, the activate command and the cache fetch command differing in cache hit information delivered during the last transfer period.

21. (Original) The system of claim 20, the cache fetch command further including way information delivered during the last transfer period.

22. (Original) The system of claim 21, the plurality of commands each delivered over four transfer periods.

23. (Original) The system of claim 22, the activate and cache fetch commands each including memory module destination information during a first transfer period.

24. (Original) The system of claim 23, the activate and cache fetch commands each including row address information during each of the four transfer periods.

25. (Currently Amended) A method, comprising:

sequentially delivering during a ~~first~~ plurality of transfer periods of a memory access transaction information corresponding to both an activate command and a cache fetch

command from a memory controller to a memory module over a plurality of command lines of a memory bus, the information being partitioned into a plurality of segments corresponding to the plurality of transfer periods and each segment being transmitted via one of the commands lines within one of the plurality of transfer periods; and

delivering from the memory controller to the memory module during a last transfer period of the plurality of transfer period associated with the memory access transaction information differentiating between an activate command and a cache fetch command.

26. (Currently Amended) The method of claim 25, wherein delivering during a last transfer period information differentiating between an activate command and a cache fetch command includes delivering one of cache way and cache hit information.

27. (Currently Amended) A method, comprising:

sequentially delivering during a ~~first~~ plurality of transfer periods information corresponding to both a read command and a read and preload command from a memory controller to a memory module over a plurality of command lines of a memory bus, the information being partitioned into a plurality of segments corresponding to the plurality of transfer periods and each segment being transmitted via one of the commands lines within one of the plurality of transfer periods; and

delivering from the memory controller to the memory module during a last transfer period of the plurality of transfer period associated with the memory access transaction information differentiating between a read command and a read and preload command.

28. (Currently Amended) The method of claim 27, wherein delivering during a last transfer period information differentiating between a read command and a read and preload command includes delivering one of cache way, eviction buffer, and cache hit information.